DeepTech Hackathon 2026

AI-Enabled Chip Design

Build breakthrough solutions for AI defect classification for semiconductor wafer/die images. Grand Finale at IESA Vision Summit 2026 (Bengaluru) — pitch to IESA leadership + top industry experts.

Organized By

Hackathon Partner

Partners

About the IESA Hackathon

The IESA DeepTech Hackathon is a national platform for building practical, industry-ready solutions in two of the most critical technology domains shaping India's electronics future: semiconductor design and embedded systems.
This hackathon is designed to do more than just collect ideas. It is structured to help teams move from a problem statement to a clear solution architecture, working prototype/demo, and a compelling pitch, supported by domain mentorship and a transparent evaluation framework.

Grand Finale at IESA Vision Summit 2026 - Bengaluru

The most promising teams will be shortlisted to pitch at the IESA Vision Summit 2026. Finalists will get the opportunity to present to IESA leadership, semiconductor and electronics industry experts, and ecosystem partners offering high visibility, strong credibility, and real opportunities to take solutions forward.

Why This Hackathon Matters

India's electronics and semiconductor ecosystem is entering a rapid growth phase, with industry demand shifting from **only coding to deep-tech building** across **silicon and embedded systems.**

As chip design complexity increases, companies are adopting **AI/ML in workflows** to accelerate verification, optimize PPA, and improve design-space exploration. In parallel, real-world products are being deployed at the **edge**, where secure, low-latency, and reliable **embedded applications** are critical.

The **IESA DeepTech Hackathon 2026** aligns directly with these trends, providing a national platform for talent to build **industry-relevant prototypes** in two future-critical tracks:

Finalist teams will showcase their solutions at the **IESA Vision Summit 2026, Bengaluru**, gaining visibility with **IESA leadership and senior industry experts,** and unlocking real next-step opportunities beyond the hackathon.

Why it matters:

01 Build talent for AI enabled embeeded/ edge, fastest-growing deep-tech skill areas.

02 Moves teams beyond ideas to working demos + measurable outcomes (benchmarks, results, documentation).

03 Creates a stronger pipeline for industry by surfacing high-signal talent and prototype-ready innovations.

04 Offers a unique advantage: Vision Summit stage access for finalists to pitch and network with the ecosystem.

Problem Statement

Edge AI–Based Defect Classification System for Semiconductor Wafer/-Die Images

Background

Semiconductor fabrication involves hundreds of tightly controlled steps. Any step can introduce microscopic defects that impact performance or cause catastrophic failures. Modern lines generate terabytes of inspection images daily, captured using tools such as optical microscopes, Scanning Electron Microscope (SEM), Atomic Force Microscope (AFM), and defect review stations.

Centralized analysis/manual review struggles due to:

- High latency
- Expensive infrastructure
- Network/bandwidth bottlenecks
- Difficulty scaling to real-time throughput

Edge-AI enables on-device defect analysis with minimal latency and reduced dependency on cloud connectivity, aligned with Industry 4.0 manufacturing environments

Problem Description

Semiconductor manufacturing produces large volumes of wafer and die inspection images. Defects in these images can reduce yield and cause failures, but traditional centralized/manual inspection creates latency, bandwidth bottlenecks, and high infrastructure cost, making it difficult to scale to real-time production needs.

Your task is to develop an Edge AI–based solution capable of detecting and classifying defects in semiconductor wafer and die images using AI/ML techniques. The design must carefully balance accuracy, latency, computational efficiency, and ease of deployment on edge based hardware.

Objective

Design and build an Edge-AI powered defect classification system capable of:

1. Detecting and classifying defects in wafer/die images into predefined categories
2. Demonstrating strong accuracy with lightweight compute (edge constraints)
3. Supporting real-time, high-volume inspection workflows by being portable to edge deployment flows (NXP eIQ)

Scope & Key Requirements

Dataset Data collection and dataset creation

- Select at least six distinct types (classes) of semiconductor manufacturing defects, ensuring that no two defect classes overlap (example defect types include shorts, opens, bridges, malformed vias, CMP scratches, cracks, LER, etc. see reference section below for sample images). In addition to these defect classes, you must also include the categories “Clean” and “Other”, resulting in a minimum total of eight classes.
- Gather images representing both clean and defective samples from any available source to build your own dataset. No dataset will be provided during the Hackathon, except during Phase 2, where a test dataset will be supplied exclusively for prediction.
- Your dataset should include a minimum of 500 images covering the clean, defective, and “Other” categories, with a well balanced distribution across classes. For better model performance, a dataset of over 1,000 images is recommended.
- Prefer using black-and-white (single channel) images; color images are not recommended.

Model Development Scope

- Use Python
- Framework: TensorFlow / PyTorch / any AI framework (allowed)
- Training approach: from scratch or transfer learning (allowed)
- Target: good accuracy + low model size + portability for edge deployment

Edge Porting Scope (Software Only)

- Port the trained model using NXP eIQ platform targeting NXP i.MX RT series devices.
- No hardware/board demo is in scope; ends at generation of deployment artifacts / bit-file output as per flow.
- Technical Support by Hackathon organizers for this step is limited to online documentation.

Documentation & Presentation Scope

- Document end-to-end approach, innovation highlights, challenges faced, and future scope.
- Present solution in a clear and structured manner (dataset → model → evaluation → edge porting → impact).

Objective

Teams must submit the following (as applicable by phase):

1. Document describing problem understanding, approach, dataset plan, model plan etc. as provided in the template. Submit a filled pdf document.
2. Dataset: single .zip file of images + class categories. Follow folder structure to group the images into Train, Validation, Test folders. Each of these folders should contain sub-folders for 'clean', 'other', 'defect class Name_1', 'defect class Name_2' … 'defect class Name_N'.
3. Trained ML Model: in ONNX format
4. Model Results (on your test set): Accuracy, Precision, Recall, Confusion Matrix, Model size, Algorithm used, platform used for training and inference.
   - Note1: If you have used GPUs/cloud infra please specify
   - Note2: Model can be built from scratch or could use pre-trained models with transfer-learning.
5. GitHub repository link (mandatory) with README complete code of development.
6. Model Results (hackathon test set): Accuracy, Precision, Recall, Confusion Matrix.
7. NXP eIQ Ported Model Results: text file of instruction stack (as per eIQ documentation)
8. Complete code (preprocessing + training + inference)
9. Final Documentation addressing the end-to-end solution covering development and learning from all the above stages.

Evaluation Data Rule

After the phase-1 submission deadline, the submitted model becomes the reference model, and no re-submission is allowed. Teams then proceed to next steps and edge-porting.

Phase	Phase 1	Phase 2	Phase 3
Who participates	All teams	Shortlisted teams for Phase 2 (30 Teams)	Finalists (10 Teams)
Goal	Register and submit the first version of the solution and approach	Validate model generalization using organizer-provided test images	Demonstrate edge readiness + deliver final pitch
What teams must submit (Deliverables)	Items #1-5 of deliverables mentioned above	Item #6 of deliverables mentioned above	Items #7-9 of deliverables mentioned above
Evaluation Criteria	Dataset Quality, size, Class balance, Model Accuracy, Model Size	Prediction Accuracy, Number of Defect classes model can classify, Model Size	Successful generation of bitfile, Size of generated model stack, Patentable concepts, Innovation Publication possibility, Methodology
Steps	1) Data Collection, Dataset creation, Proposed Methodology 2) AIML model development	1) Prediction using Hackathon Supplied 'Test Dataset'	1) Model Porting and Optimization for Edge-AI 2)Presentation, Documentation

Remarks

a. The hackathon is aimed at an intermediate development level, positioned between a prototype and a fully functional solution. Participants are encouraged to explore diverse ideas and demonstrate creativity in how they approach the challenge.
b. During Phase #1 above, it would be good to prepare for phase #3 by pre-visiting requirements for phase #3 to ensure compatibility, portability, model conversion formats etc.
c. For phase #3 No hardware boards will be provided as part of hackathon. It ends with generation of bit-file. Support for Phase #3 is limited to the online documentation already available. No additional support will be provided.

References

NXP eIQ documentation:

- https://www.nxp.com/design/design-center/software/eiq-ai-development-environment/eiq-toolkit-for-end-to-end-model-development-and-deployment:EIQ-TOOLKIT
- Sample images and document - Defect Classification System for Semiconductor Sample Images

Hackathon Timeline

19-Jan-26

Registrations Open (Only Registration)

Team registrations go live. Create your team and complete registration early so you're ready when problem statements are revealed.

21-Jan-26

Problem Statements Revealed

Official problem statements are published. Review problem statement and start planning your approach.

23- Jan- 2026

Orientation Session (Online)

Join the official orientation to understand the problem statement, objective and delivery, hackathon flow, submission format, evaluation criteria, and tips to build a strong entry.

28 Jan 26

Webinar / Q&A session 1

Join quick interactive webinars to understand the concept and get clarification on doubts.

04 Feb 26

Webinar / Q&A session 2

Join quick interactive webinars to understand the concept and get clarification on doubts.

08 Feb 26

Phase 1 Submission Closes

Final deadline for Phase 1 idea submission. Make sure your entry follows the template and is complete.

11 Feb 26

Announcement of Semi-Finalists (Phase 2 Teams)

Selected teams for Phase 2 will be announced on email/portal. Next-step instructions and Phase 2 requirements will be shared.

12 Feb 26

Phase 2 Kickoff Session (30 Selected Teams Only)

Mandatory online session for Phase 2 teams realted to deliverables & expectations

18 Feb 26

Phase 2 Submission Closes

Submit Phase 2 deliverables.Final deadline for Phase 2 submissions. No changes accepted after this.

19 Feb 26

Finalists Announcement (Top Teams for Grand Finale)

Finalists are announced and onboarded for the Vision Summit Grand Finale. Travel and venue instructions will be shared.

21 Feb 26

Mentoring for Finalists (Closed Sessions)

Focused mentoring to polish the solution, strengthen demo readiness, and finalize the pitch deck.

24–25 Feb 2026

Team Arrival & Venue Onboarding (Bengaluru)

Finalists arrive, check-in, and settle. Venue orientation, tech checks, and schedule briefing (as per summit plan).

25–26 Feb 2026

Grand Finale @ IESA Vision Summit 2026 (Bengaluru)

Finalists pitch on the Vision Summit stage to IESA leadership and senior industry experts. Winners are announced with prizes and next-stage opportunities.

Prizes and Rewards

1st RUNNERUP

₹ 60,000

WINNER

₹ 1,00,000

2nd RUNNERUP

₹ 40,000

Beyond Cash — What Finalists Get

01 Access to IESA Vision Summit 2026 (Bengaluru): Finalists get the opportunity to attend the summit and pitch on a high-visibility stage in front of IESA leadership and senior industry experts.

02 Sponsor Kits & Tool Benefits: Exclusive hardware / development kits, tool credits, and goodies from sponsoring partners (subject to sponsor availability).

03 High-Value Networking: Direct networking with industry leaders, semiconductor & embedded experts, startups, and ecosystem partners at the summit.

04 Internship & Job Opportunities: Top teams get visibility for internships, hiring opportunities, and project collaborations with participating companies and partners.

05 Recognition & Visibility: Certificates, digital badges, and feature highlights across IESA + i4C channels for top teams.

About IESA

IESA is India's leading industry body for ESDM, semiconductors, and intelligent electronics, connecting industry, startups, academia, and policymakers to strengthen India's innovation and manufacturing ecosystem.

About IESA Vision Summit 2026

IESA Vision Summit 2026 is IESA's flagship industry gathering focused on advancing India's semiconductor and electronics (ESDM) ecosystem bringing together industry leaders, policymakers, startups, academia, and technology experts for strategic discussions, partnerships, and showcases. The 2026 theme is "Design to Manufacturing — Synergy of Product, Production and Skill", emphasizing India's transition toward a Product Nation, Production Nation, and Skills Nation.

25–26 Feb 2026

The Leela Bhartiya City Convention Centre, Bengaluru, India.

2000+	60+	20	6+	25+
Delegates	Exhibitors	Keynotes	Panel Discussions	Sessions

About i4C

i4C (Inter Institutional Inclusive Innovations Centre) is a national innovation and Hackathon-as-a-Service partner working with government bodies, industry, startups, and academic institutions. i4C designs and executes high-impact hackathons, innovation programs, and upskilling initiatives that help identify talent, validate ideas, and build real-world, deployable solutions.

Frequently Asked Questions

Who can participate?
Students, Btech, BE, PhD, research fellow.

What is Team size?
2–4 members (recommended).

Online or offline?
Development is online; Grand Finale at IESA Vision Summit 2026, Bengaluru.

What to submit?
Deck + demo/prototype + documentation + repo/video (as applicable).

Do we need to buy hardware?
For embedded track, teams may use their own dev boards and hardware.

What's the evaluation basis?
Innovation, feasibility, technical depth, impact, demo quality.

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DeepTEch Hackathon Update

Scan this QR code to join this group

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